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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,043	06/19/2003	Kiyong Choi	004735.P004	6395

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EXAMINER

SHINGLETON, MICHAEL B

ART UNIT PAPER NUMBER

2817

DATE MAILED: 12/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/600,043	Applicant(s) CHOI ET AL.	
	Examiner Michael B. Shingleton	Art Unit 2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10/17/2005
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 2 and 4-12 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1 and 9-11 is/are allowed.
- 6) ☒ Claim(s) 2, 4-8 and 12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received

Michael B. Shingleton
MICHAEL B. SHINGLETON
PRIMARY EXAMINER
(4001) PART 1 UNIT 2817

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2, 4, 7, 8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Afrashteh 5,426,641 (Afrashteh) in view of Ferris 4,591,774 (Ferris).

Figure 2 and the relevant text of Afrashteh disclose a method for operating a RF power amplifier 203. A digital signal 213 is applied to the RF power amplifier 203 via the elements 212 and 204. The term program is directed to “a plan or system under which action may be taken toward a goal” accordingly the programming a conduction angle is the action of achieving that goal. The gate bias control circuit 204 thereby programs the conduction angle of the RF power amplifier using the digital signal 213 or in other words this circuit provides for the programming a conduction angle to the RF power amplifier with the digital signal 213. Since no specific definition is provided by the applicant, the examiner must give the broadest reasonable interpretation to these terms (See MPEP 2111 and 2111.01). Also note that an analog information signal 201 is applied to the RF power amplifier as is clearly illustrated by Afrashteh. Also clearly the RF power amplifier 203 is operated at the conduction angle specified by the digital signal 213. The above arrangement clearly provides for a digital control function coupled to the RF power amplifier. Afrashteh is silent on the D/A converter as being composed of a plurality of inverters and specifically CMOS inverters.

Figure 5 and the relevant text of Ferris discloses a conventional D to A converter that includes a plurality of buffers. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the D to A converter of Afrashteh with one that includes a plurality of inverters because as the Afrashteh is silent on the exact structure of the D to A converter, one of ordinary skill in the art would have been motivated to use any art-recognized equivalent D to A converter circuit such as the conventional D to A converter D to A converter as taught by Ferris.

Both Afrashteh and Ferris are silent on the specific structure of the inverters as shown as element 44 in Ferris. However, CMOS inverter structures are an art recognized equivalent and conventionally

known inverter structure. CMOS means that there are both PMOS and NMOS transistors. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the inverter Afrashteh and Ferris with one that includes a plurality of inverters because as the Afrashteh and Ferris references are silent on the exact structure of the inverters, one of ordinary skill in the art would have been motivated to use any art-recognized inverter structure including the conventional CMOS inverter.

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Afrashteh 5,426,641 (Afrashteh) in view of Ferris 4,591,774 (Ferris) as applied to claims 2, 4, 7, 8 and 12 above, and further in view of Sowlati US2002/0196086 (Sowlati).

Afrashteh and Ferris as applied above in the rejection of claim 2, 4, 7 and 12 and the following: Afrashteh and Ferris are silent on the details of the RF power amplifier.

Self-biased cascode stage amplifiers are conventional in the art for use as RF power amplifiers. Sowlati shows various cascode stage self-biased power amplifiers in Figures 3a-c, 4a-b, 5a-b and Figure 6. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the RF power amplifier of Afrashteh with a self-biased cascode stage RF power amplifier because, as the Afrashteh reference is silent on the exact RF power amplifier stage employed one of ordinary skill in the art would have been motivated to use any art-recognized equivalent RF power amplifier stage therefore such as the conventional self-biased cascode differential stage RF power amplifier as shown by Sowlati.

Afrashteh is also silent on the employment of a driver stage prior to the RF power amplifier stage. This is common-place in the art so as to allow for signals of “smaller” magnitude to power the RF power amplifier.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ a driver stage prior to the RF power amplifier stage so as to allow signals smaller than could power the RF amplifier by themselves to power the RF power amplifier as is conventionally known in the art.

Afrashteh and Sowlati are both silent on the forming of a cross-coupling the differential stage amplifier. However, cross-coupling in differential amplifier arrangements is conventional known so as to improve linearization. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have cross-coupled the arrangement of Afrashteh and Sowlati so as to improve linearization as is conventionally known in the art.

Claims 1, and 9-11 are allowable over the prior art of record.

Response to Arguments

Applicant's arguments filed 11-21-2005 have been fully considered but they are not persuasive.

Firstly the interview that was held prior to this office action apparently did not get scanned into the file. The examiner requests the date of that interview so that the examiner can reconstruct the file.

During the above interview the claim language of programmed was discussed. And the proposed claim language relating to the strengths of the inverters were discussed. Upon looking at the amendment the prior art the examiner contends that it does not overcome the rejection of the previous office action and this rejection is still applied above. In particular the strengths of the inverters 44 of Ferris are changed from zero to one or from one to zero and in accordance with this digital signal formed from the digital signal from the microprocessor, the element 46 converts the digital to the analog. In effect the inverter arrangement like 532, 534, 542, 544, 552, 554 of the instant invention forms the function of an Digital to analog converter. It takes the digital signal and converts this to an analog bias voltage. Therefore the function recited does not overcome the combination made obvious above for it is a basic function of the D/A converter of Ferris. The D/A converter of Afrashteh is replaced with one that incorporates inverters. More structure is needed in order to overcome the rejection and Applicant is invited to call the examiner in hopes that some language can be agreed to that will overcome the art of record.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 and after July 15, 2005 the fax number will be 571-273-8300. Note that old fax number (703-872-9306) will be service until September 15, 2005.

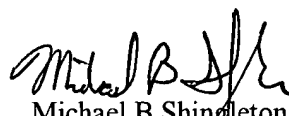
Art Unit: 2817

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS

June 27, 2005

December 25, 2005


Michael B Shingleton
Primary Examiner
Group Art Unit 2817